CLAIMS

What is claimed is:

1. A method of forming a capacitor in a ferroelectric random access memory (FeRAM) on a semiconductor wafer, the semiconductor wafer comprising a substrate, and an insulation layer positioned on the substrate, the method comprising:

forming a bottom electrode on the insulation layer;

forming a dielectric layer on the semiconductor wafer covering the bottom electrode;

performing an etching process to form an upper electrode hole in the dielectric layer through to the surface of the bottom electrode;

forming a spacer around the walls within the upper electrode hole;

forming a capacitor dielectric layer on the surface of the dielectric layer, on the bottom within the upper electrode hole, and on the spacer; and

forming an upper electrode in the upper electrode hole.

2. The method of claim 1 wherein the bottom electrode is composed of noble metals consisting of platinum (Pt), palladium (Pd), iridium (Ir), rhodium (Rh), osmium (Os), or ruthenium (Ru).

3. The method of claim 1 wherein the bottom electrode is composed of both a platinum layer and a titanium layer, or is composed of a platinum layer, an iridium dioxide (IrO_2) layer and an iridium layer.

4. The method of claim 1 wherein the capacitor dielectric layer is composed of lead zirconate titanate (PZT).

5. The method of claim 1 wherein the dielectric layer is composed of both a silicon dioxide layer and a titanium dioxide (TiO_2) layer.

6. The method of claim 5 wherein the spacer is composed of titanium dioxide, and is used to prevent the capacitor dielectric layer formed of PZT from reacting with the silicon dioxide layer.

7. The method of claim 1 wherein the upper electrode is composed of iridium dioxide.

8. The method of claim 1 wherein the upper electrode comprises of platinum (Pt), copper (Cu), aluminum (Al), titanium (Ti), or titanium nitride (TiN).

9. A method of enhancing the qualities of a capacitor dielectric layer in a capacitor in a ferroelectric random access memory (FeRAM) on a semiconductor wafer, the semiconductor wafer comprising a substrate, and an insulation layer positioned on the substrate, the method comprising:

forming a bottom electrode on the insulation layer;

forming a silicon dioxide layer on the semiconductor wafer covering the bottom electrode;

forming a titanium dioxide (TiO_2) layer on the silicon dioxide layer;

performing an etching process to form an upper electrode hole in the titanium dioxide layer and the silicon dioxide layer through to the surface of the bottom electrode;

forming a spacer of titanium dioxide around the walls within the upper electrode hole;

forming the capacitor dielectric layer of lead zirconate

titanate (PZT) on the surface of the titanium dioxide layer, on the bottom within the upper electrode hole, and on the spacer; and

forming an upper electrode in the upper electrode hole;

wherein the titanium dioxide layer and the spacer composed of titanium dioxide are both used to prevent the capacitor dielectric layer formed of PZT from reacting with the silicon dioxide layer so as to prevent the capacitor dielectric layer from cracking or lifting.

10. The method of claim 9 wherein the bottom electrode is composed of noble metals consisting of platinum (Pt), palladium (Pd), iridium (Ir), rhodium (Rh), osmium (Os), or ruthenium (Ru).

11. The method of claim 9 wherein the bottom electrode is composed of both a platinum layer and a titanium layer, or is composed of a platinum layer, an iridium dioxide (IrO_2) layer and an iridium layer.

12. The method of claim 9 wherein the upper electrode is composed of iridium dioxide.

13. The method of claim 9 wherein the upper electrode comprises of platinum (Pt), copper (Cu), aluminum (Al), titanium (Ti), or titanium nitride (TiN).